REMARKS/ARGUMENTS

Claims 1-12 were previously pending in the application. Claim 1 is amended; and new claims 13-16 are added herein. Assuming the entry of this amendment, claims 1-16 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 1 of the office action, the Examiner objected to the drawings because Fig. 8 does not have label **804** for the noise-shaping loop. In response, the Applicant notes that the copy of Fig. 8 in Applicant's prosecution file does have label **804** located at the top right corner of the box containing the noise-shaping loop circuitry. Furthermore, the Applicant submits herewith a Transmittal of Formal Drawings, with Fig. 8 having label **804**.

In paragraph 2, the Examiner rejected claims 1, 3, and 12 under 35 U.S.C. § 102(e) as being anticipated by Savelli. In paragraph 3, the Examiner rejected claims 5, 6, 8, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Savelli in view of Perrott. In paragraph 4, the Examiner rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Savelli in view of Perrott, and in further view of Riley. In paragraph 5, the Examiner objected to claims 2, 4, 10, and 11 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form.

For the following reasons, the Applicant submits that all claims are allowable over the cited references.

Claims 1-12:

Support for the amendment of claim 1 can be found, e.g., in Applicant's Fig. 2. Amended claim 1 is directed to a frequency synthesizer for generating a data-modulated output signal based on a reference signal and an input data signal. The frequency synthesizer has (a) a phase-locked loop (PLL) circuit; (b) a first data-modulation path; and (c) a second data-modulation path. The PLL circuit is configured to receive the reference signal and generate the data-modulated output signal. The first data-modulation path is configured to (i) generate a first data-modulated input signal based on the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator (VCO) of the PLL circuit. The second data-modulation path is configured to (i) generate a second data-modulated input signal based on the input data signal and (ii) provide the second data-modulated input signal at a frequency divider of the PLL circuit to control the divider's division factor.

Savelli discloses a PLL-based frequency synthesizer, which is shown in his Fig. 2. More specifically, Savelli's frequency synthesizer has: (a) a PLL circuit having phase comparator **7**, loop filter **5**, VCO **1**, and counter-divider **8**, which is a part of a feedback path connecting the VCO and the phase comparator; (b) data-modulation branch **34** having circuit elements **38** and **40**; and (c) compensation branch **36** having circuit elements **52-68**. Based on an input data signal (applied to the frequency synthesizer at circuit element **30**), data-modulation branch **34** generates a data modulated signal, which is then applied to VCO **1** to generate a data-modulated output signal (f0). Compensation branch **36** processes the data-modulated output signal generated by VCO **1** to remove the data modulation (see, e.g., col. 7, lines 47-55) and applies the resulting unmodulated signal to counter-divider **8** as a feedback signal (see, e.g., Savelli's Fig. 2). The Applicant submits that Savelli does not teach or suggest that a data-modulated signal can be applied to counter-divider **8** as to control the divider's division factor, as explicitly recited in amended claim 1.

Perrott discloses a PLL-based frequency synthesizer, which is shown in his Fig. 2A. More specifically, Perrott's frequency synthesizer has: (a) a PLL circuit having phase-frequency detector (PFD) **36**, loop filter **40**, VCO **26**, and multi-modulus divider **30**, which is a part of a feedback path connecting the VCO and the PFD; and (b) a data modulation path having circuit elements **46**, **50**, and **56**. The data-modulation path generates data-modulated signal **58**, which is applied to multi-modulus divider **30** as a signal that controls the divider's division factor.

First of all, the Applicant notes that Perrott teaches a single data-modulation path and, as such, the teachings of Perrott in and by themselves are insufficient for rejecting claim 1, which explicitly recites first and second data-modulation paths.

Second, the Applicant submits that neither Savelli nor Perrott has a suggestion that would lead one skilled in the art to combine the teachings of these two references together. More specifically, there is no teaching or suggestion in Savelli that the signal (labeled N in Savelli's Fig. 2) controlling the division factor of counter-divider **8** can be data modulated. Similarly, there is no teaching or suggestion in Perrott that, in addition to applying a (first) data-modulation signal to multi-modulus divider **30**, VCO **26** can receive another (second) data-modulated signal. Moreover, Perrott specifically teaches that data-modulating the division factor of the PLL's frequency divider is an alternative (not a complement) to data-modulating the PLL's VCO (see, e.g., Perrott's col. 2, line 39, through col. 3, line 30). As such, Savelli and Perrott effectively teach away from combining their respective modulation techniques and/or circuits.

Finally, even if Savelli and Perrott had a suggestion for somehow combining their frequency synthesizers, which the Applicant does not admit, the resulting combination circuit would fail to function. More specifically, Savelli's frequency synthesizer requires that the feedback signal applied to counter-divider **8** be free of data modulation "[i]n order not to pollute the signal in the feedback loop **9** with the modulation at the output of the VCO **1**, and to guarantee that the synthesized frequency is highly stable" (Savelli's col. 6, lines 63-65). In contrast, Perrott's frequency synthesizer is specifically designed to use the data-modulated output signal generated by VCO **26** as the feedback signal at multi-modulus divider **30** and to function without any feedback compensation circuitry (see Perrott's Fig. 2A and the paragraph beginning at col. 2, line 55). Thus, removing data-modulation from the feedback signal (as in Savelli's frequency synthesizer) would destroy the functionality of Perrott's frequency synthesizer. Alternatively, having data modulation in the feedback signal (as in Perrott's frequency synthesizer) would render the PLL in Savelli's frequency synthesizer unstable. To summarize, due to the above-outlined differences in the properties of their respective feedback signals, the frequency synthesizers of Savelli and Perrott are not compatible with one another.

Riley discloses a frequency synthesizer that is not PLL-based. The Examiner does not contend that Riley teaches any limitations of original claim 1, all of which are present in amended claim 1.

For all these reasons, the Applicant submits that amended claim 1 is allowable over the cited references. Since claims 2-12 depend variously from claim 1, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under §§ 102 and 103 have been overcome.

Claims 13-16:

Claim 13 is equivalent to original claim 2 rewritten in independent form. Since original claim 2 was indicated as allowable, the Applicant submits that claim 13 is allowable.

Claim 14 is equivalent to original claim 4 rewritten in independent form. Since original claim 4 was indicated as allowable, the Applicant submits that claim 14 is allowable.

Claim 15 is equivalent to original claim 10 rewritten in independent form. Since original claim 10 was indicated as allowable, the Applicant submits that claim 15 is allowable. Since claim 16, which is equivalent to original claim 11, depends from claim 15, it is further submitted that claim 16 is also allowable.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Yuri Gruzdkov
Registration No. 50,762
Agent for Applicant
(215) 557-8544 (phone)
(215) 557-8477 (fax)